# Kevin Nakamura

FAILURE ANALYSIS ENGINEER

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## SUMMARY

Failure analysis engineer with 4 years in semiconductor device analysis, from electrical fault isolation to physical failure analysis with SEM, FIB and X-ray. Closes about 25 customer and reliability cases a quarter with root cause analysis that fabs and design teams act on. Writes clear reports and automates lab data work in Python, SQL and JMP.

## SKILLS

Failure Analysis • Fault Isolation • Physical Failure Analysis • SEM/EDX • FIB • X-Ray • Oscilloscopes
Root Cause Analysis • Python • JMP

## EXPERIENCE

**Failure Analysis Engineer** 02/2024 - Present

Capitol Silicon Devices Austin, TX

*Failure analysis lab supporting a mixed-signal chip maker's customer returns and reliability qualifications.*

- Run fault isolation on **25+** returned devices a quarter using curve tracers, oscilloscopes, power supplies and thermal imaging.
- Perform physical failure analysis with decapsulation, cross-sections, FIB cuts and SEM/EDX to find defect sites.
- Lead root cause analysis with fab and design teams, cutting repeat failure modes on one product line by 40%.
- Develop Python and SQL scripts that pull test data into JMP, saving about 6 hours of analysis per case.
- Present findings to customers in 8D reports, with 95% of cases closed inside the 30-day target.

**Product Engineer** 07/2022 - 01/2024

Hill Country Microelectronics Round Rock, TX

*Test and product engineering for power management ICs.*

- Analyzed wafer sort and final test yield in JMP for 6 power management products.
- Debugged test programs with logic analyzers and bench power supplies, raising final test yield from 91% to 96%.
- Coordinated X-ray and acoustic microscopy checks with the package house on 14 assembly lots.
- Wrote failure analysis requests with electrical data so the lab could start within 24 hours.

## EDUCATION

**Bachelor of Science** 05/2022

The University of Texas at Austin Austin, TX

Electrical Engineering